AMENDMENTS TO THE DRAWINGS

Please replace the drawings on file with the formal drawing sheets submitted herewith. The only changes to the drawings are that Figure 9 has been labelled as "Prior Art" as required. An annotated copy of Figure 9 is included to show the changes.

REMARKS

Claims 1-16 are pending. The drawings have been amended to label Figure 9 as prior art, as required. Favorable reconsideration is respectfully requested.

Claims 1 and 13 were rejected under 35 U.S.C. 103 over the prior art of Applicant's Figure 9 in view of U.S. Patent 6,097,712 (Secord et al.). Claims 2 and 14 were rejected under 35 U.S.C. 103 over the prior art of Applicant's Figure 9, presumably in view of Secord et al., and further in view of U.S. Patent 6,625,199 (Secord et al.). Applicant traverses as follows.

Claim 1 is directed to a synchronous acquisition device for a CDMA receiver that receives as a receiver signal a signal transmitted by spectrum-spreading transmission data including one of first to mth pieces (m: an integer 2 or more) of fixed data using a spreading code, having a plurality of paths into which the receiver signal is branched.

Each of the paths includes: a first multiplier for multiplying the receiver signal by the spreading code; a first integrator for integrating an output signal of the first multiplier by one-symbol-time; fixed data sequential output units for having the first to mth pieces of fixed data and sequentially outputting the first to mth pieces of fixed data; a second multiplier for multiplying an output signal from the first integrator by the first to mth pieces of fixed data outputted from the fixed data sequential output units, and sequentially outputting first to mth multiplication results; correlation value sequential output units for sequentially outputting the first to mth multiplication results as first to mth correlation values; and a path-corresponding maximum value detector for detecting a maximum value of the first to mth correlation valuesinter alia, second multiplier that multiplies the output of the first integrator by the first to mth pieces of fixed data outputted from fixed data sequential output units, and sequentially outputs first to mth multiplication results, which are then sequentially output as first to mth correlation values by correlation value sequential output units.

In the Office Action, the position was taken that the difference between the admitted prior art of Figure 9 and the claimed invention was that "the prior art differs in structure from applicant's claimed arrangement in 1st and 2nd integrators."

However, the prior art of Figure 9 requires m integrators 12', one for each of the products of spreading code c(t) and fixed data $X_1(t) \ldots X_m(t)$. On the other hand, due to the advantageous structure defined in claim 1, and as shown in one exemplary embodiment in Figure 1, in the applicant's invention, the design is simplified so that a single integrator (e.g., 12) can be used to perform the function that required m integrators in the prior art of Figure 9. As can be seen from the foregoing, the differences between the present invention and the admitted prior relate to more than just the "arrangement in 1st and 2nd integrators."

In fact, the advantageous design of the invention defined in claim 1 leads to reduction in circuitry by, inter alia, permitting in the disclosed embodiment, the adder 16 in the integrator 12 to be shared. For at least the foregoing reasons, the invention of claim 1 is quite different from that shown in Figure 9.

After characterizing the Examiner's view of the differences between claim 1 and Figure 9, the Office Action noted that Secord et al. discloses CDMA receiver circuitry including multipliers and integrators. However, no allegation was made that Secord et al. remedies the deficiencies of Figure 9, even as those deficiencies are characterized in the Office Action. The Office Action then goes on to say that

> "Secord also shows additional configurations with integrators positioned between multipliers (see figures 6 and 7). As applicant's admitted prior art and Secord disclose variation of the components and functions, it appears that the components and location do not appear to require a fixed configuration and therefore the rearrangement of known components is considered to be obvious to one of ordinary skill in the art." Office Action at page 3.

To establish a prima facie case of obviousness requires, among other things, that the prior art, alone or in combination, teach or suggest *each and every element of the claim* in question. In this case, there is not even an attempt to show an actual correspondence between the elements of the cited prior art and the limitations of claim 1. For this reason alone, no prima facie case of obviousness has been established.

As discussed above, the Office Action has inaccurately characterized the differences between Figure 9 and the structure defined in claim 1. Moreover, no showing has been made that even those differences are remedied by Secord et al.

Moreover, instead of meeting each and every element of claim 1, the Office Action in effect says that because there "appear" to be many ways of mixing components to perform the function of a correlation value generation unit, then no particular combination of components, i.e., no particular design, for a correlation value generation unit can ever be patentable. Following this rule of law would make it impossible to patent almost any circuit, since various combinations of components, e.g., resistors, transistors, op amps, would generally have been previously used, in different ways, to perform the same function.

Of course, this is entirely improper as a grounds for an obviousness rejection. The Examiner is required in establishing a prima facie case of obviousness to explain how each and every element is shown or suggested in the prior art. In this case, this requirement has not even been alleged. For at least this reason, no prima facie case of obviousness has been established.

In summary: (1) the Office Action fails to show an appreciation of the differences between the applicant's invention and the prior art Figure 9; (2) the Office Action has not explained how Figure 9 and Secord et al., even when combined, actually meet the specific limitations of claim 1; and (3) the Office relies upon a rationale for determining obviousness

that is completely improper, namely, that if many ways are possible to design a circuit, then no particular way is patentable. This is clearly not the law and cannot form the basis for a rejection.

For at least the foregoing reasons, no prima facie case of obviousness has been set forth in connection with claim 1. Independent claim 13 is a method claim that recites a substantially similar feature and is believed patentable for substantially similar reasons.

The other claims in this application are each dependent from one or another of the independent claims discussed above and are therefore believed patentable for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual reconsideration of the patentability of each on its own merits is respectfully requested.

In view of the above amendment and remarks, applicant believes the pending application is in condition for allowance.

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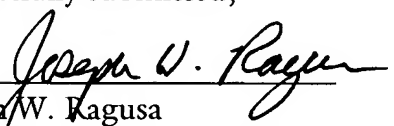
Respectfully submitted,

By 

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PRIOR ART

FIG. 9